Progressive Network-Flow Based Power-Aware Broadcast Addressing for Pin-Constrained Digital Microfluidic Biochips

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ABSTRACT

In recent emerging marketplace, designs for pin-constrained digital microfluidic biochips (PDMFBs) have received much attention due to the large impact on packaging and product cost. One of the major approaches, *broadcast addressing*, reduces the pin count by assigning a single control pin to multiple electrodes with mutually-compatible control signals. Prior works utilize this addressing scheme by minimally grouping electrode sets with non-conflict signal merging. However, merging control signals also introduces redundant actuations, which potentially cause a high power-consumption problem. Recent studies on PDMFBs have indicated that high power consumption not only decreases the product lifetime but also degrades the system reliability. Unfortunately, this power-aware design concern is still not readily available among current design automations of PDMFBs. To cope with these issues, we propose in this paper the *first* power-aware broadcast addressing for PDMFBs. Our algorithm simultaneously takes pin-count reduction and power-consumption minimization into consideration, thereby achieving higher integration and better design performance. Experimental results demonstrate the effectiveness of our algorithm.

Categories and Subject Descriptors

B.7.2 [**Integrated Circuits**]: Design Aids

General Terms

Algorithms, Performance, Design

Keywords

Digital microfluidics, electrode addressing, power

1. INTRODUCTION

As the microfluidic technology advances, digital microfluidic biochips (DMFBs) have attracted much attention recently. These miniaturized and automated DMFBs provide various advantages including high portability, high throughput, high sensitivity, high immunity to human intervention, and low sample volume consumption. Due to these advantages, more and more practical applications such as infant health care, point-of-care disease diagnostics, environmental toxin monitoring, and drug discovery have been successfully realized on DMFBs [2, 5, 11].

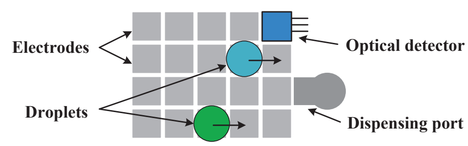

Figure 1: Schematic view of a digital microfluidic biochip.

Typically, a DMFB consists of a two dimensional (2D) electrode array, optical detector, and dispensing port, as schematically shown in Figure 1 [5]. In performing fluidic-handling functions, droplet-based operations are introduced on DMFB platforms. By generating electrohydrodynamic forces from electrodes, droplets can be dispensed from dispensing ports, moved around the 2D array for performing reactions (e.g., mixing or dilution), and then moved toward the optical detector for detection [10]. The entire operations are also called *reconfigurable* operations due to their flexibility in area and time domain [1].

In realizing fluidic controls, a primary issue is the control scheme of electrodes. To correctly control the electrodes, *electrode addressing* is introduced as a method through which electrodes are assigned by control pins to identify input signals. Early DMFB designs relied on *direct addressing*, where each electrode is directly and *independently* assigned by a dedicated control pin [4], as illustrated in Figure 2(a). This addressing maximizes the flexibility of electrode controls. However, for large arrays, the high pin-count demand complicates the electrical connections between the chip and the external controller, thus rendering this kind of chip unreliable and prohibitively expensive to package and manufacture [4, 5, 13, 14].

Recently, *pin-constrained* DMFBs (PDMFBs) have raised active discussions to overcome this problem. One of the major approaches, *broadcast addressing*, provides high throughput for bioassays and reduces the number of control pins by identifying and connecting them with *compatible* control signals. In other words, multiple electrodes are controlled by a single signal source and are thus actuated simultaneously, as shown in Figure 2 (b). In this regard, much on-going effort has been made to group sets of electrodes that can be driven uniformly without introducing any signal conflict [9, 13, 14].

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Although broadcast addressing serves as a promising solution to pin-constrained designs, yet the redundant actuations during signal merging have potentially caused a power-consumption problem. For example, in Figure 2(a), the direct-addressing result needs two exact actuations for moving the two droplets in this time step. In Figure 2(b), after applying the broadcast addressing, the pin count is greatly reduced from 20 to 7. Nevertheless, the addressing result needs two exact actuations, plus two *redundant* actuations, for moving the two droplets. As electrodes are controlled in a series of time steps, if control pins are not carefully assigned to electrodes, the addressing result will introduce a great number of redundant actuations. Hence, executing a bioassay may incur a high power-consumption problem [15].

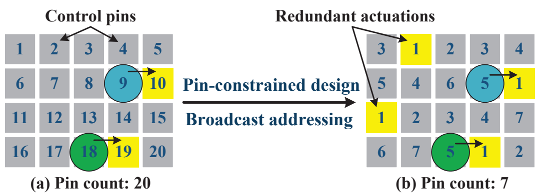

Figure 2: Moving two droplets in a specific time step. (a) A direct-addressing result uses two pins (pin 10 and pin 19) to generate two exact actuations. (b) A broadcast-addressing result uses one pin (pin 1) to generate two exact actuations, plus two redundant actuations.

As reported in recent studies, the power-consumption problem is especially critical for battery-driven applications, such as hand-held devices for point-of-care diagnosis and battery-operated sensors for environmental monitoring [2, 15]. Since these applications often require longer execution time, it is desirable to minimize the power consumption for longer battery lifetime. Besides, high power consumption reveals a fact of excessive actuations, which accelerates the dielectric breakdown of some electrodes. Such defects may result in unexpected executions and thus degrade the system reliability [1, 5].

Unfortunately, current broadcast addressing for PDMFBs neglects the induced number of redundant actuations during signal merging and pin sharing, which causes a significant power-consumption problem. As reported in [13], even the simplest broadcast addressing with pin-count minimization has been presented as NP-hard. And thus the design convergence imposed by simultaneously minimizing the pin count and power consumption has become the most difficult challenge. Due to the distinct nature from traditional VLSI technology, a specialized tool must be developed to solve this problem efficiently and effectively such that PDMFBs can be more feasible for practical applications.

1.1 Our Contributions

In this paper, we propose the *first* power-aware broadcast addressing for PDMFBs. By considering both pin-constrained and power-aware design issues, our algorithm can simultaneously minimize the pin count and power consumption to achieve high design performance. The contributions of this paper are summarized as follows.

- We introduce a new problem formulation of power optimization for broadcast-addressing PDMFBs. We also propose the *first* addressing algorithm to minimize the power consumption while considering the pin-count reduction.
- Unlike typical broadcast addressing which only deals with the compatibility for identical signals, our work can handle the integration between identical and complementary signals simultaneously. In this regard, further pin-count reduction can be achieved.
- Motivated from [6], we propose a progressive addressing algorithm based on a *minimum-cost maximum-flow* network to efficiently solve the entire power-aware addressing problem.

Experimental results demonstrate the effectiveness of our addressing algorithm. The evaluation performed on a set of real-life chip applications shows that our addressing algorithm achieves the best results in terms of pin count and power consumption.

The remainder of this paper is organized as follows. Section 2 describes the related preliminaries and formulates the design problem. Section 3 details the proposed power-aware broadcast-addressing algorithm. Finally, sections 4 and 5 show our experimental results and conclusion.

2. DESIGN FOR POWER-AWARE PDMFBS

In this section, we introduce the related background of power-aware pin-constrained design. In the beginning, we show the functions of broadcast addressing and indicate the power-consumption problem. Then, we formulate the power-aware pin-constrained design problem.

2.1 Broadcast Addressing

To execute a specific bioassay on a DMFB, information for fluidic controls must be stored in the form of *electrode actuation sequences*. Each bit in the sequence represents the actuation status of the electrode in a specific time step, and can be represented as actuated "1", de-actuated "0", or don't care "X". The term "1" ("0") represents a control signal with a relatively logic-high (logic-low) value of the actuation voltage. The symbol "X" indicates that the input signal can be either "1" or "0", which has no impact on scheduled fluidic controls [13]. Figure 3(a) gives an example of an electrode set and the corresponding actuation sequences.

To correctly drive these electrodes, control pins must be appropriately assigned to electrodes for identifying input signals. This manner is also referred to as *electrode addressing*. In pin-constrained chip designs, broadcast addressing focuses on electrode grouping and control signal merging by identifying the signal compatibility. Specifically, each electrode actuation sequence may contain several don't care terms. By carefully replacing these don't care terms with "1" or "0", multiple actuation sequences can be merged to an *identical* outcome, which is also referred to as the *common compatible sequence* of these electrodes. Hence, these electrodes can share the same control pin to receive the same control signal thereby reducing the pin count. Take electrodes e_4 and e_5 in Figure 3(a) for example. By replacing "X" in the actuation sequence of e_4 with "1", we can merge the actuation sequences of e_4 and e_5 to an identical outcome "01001". Therefore, e_4 and e_5 can be addressed with the same control pin due to their mutually compatible actuation sequences. Figure 3(b) shows a broadcast addressing result with 5 required control pins.

Electrode	e_1	e_2	e_3	e_4	e_5	e_6	e_7	e_8	e_9	e_{10}	e_{11}	e_{12}
Actuation sequence	1 0 0 X X	1 0 0 X X	0 1 0 0 X	0 1 0 0 X	0 1 0 0 1	1 0 X 1 X	1 0 X 1 X	0 1 0 0 1	X X 0 1 X	X X 0 1 X	0 1 1 X X	0 1 1 X X

(a)

Addressing result

Pin	Electrode group	Outcome actuation sequence
1	e_1, e_2	1 0 0 1 1
2	e_{11}, e_{12}	0 1 1 1 1
3	e_6, e_7	1 0 1 1 1
4	e_3, e_4, e_5, e_8	0 1 0 0 1
5	e_9, e_{10}	1 1 0 1 0

(b) Pin count: 5 #RAUs: 18

Addressing result

Pin	Electrode group	Outcome actuation sequence
1	e_1, e_2	1 0 0 1 1
	e_{11}, e_{12}	0 1 1 0 0
2	e_6, e_7	1 0 1 1 0
	e_3, e_4, e_5, e_8	0 1 0 0 1
3	e_9, e_{10}	0 0 0 1 0

(c) Pin count: 3 #RAUs: 8

Figure 3: (a) An electrode set and the corresponding sequences. (b) Previous power-oblivious broadcast addressing with considering the compatibility only for identical signals, which requires high pin count and high power consumption. (c) Our power-aware broadcast addressing with considering the compatibility between identical and complementary signals, which achieves low pin count and low power consumption.

Although the typical broadcast addressing can alleviate the rapid growth of pin-count demand, the only consideration for identical signals restricts the solution quality of pin-constrained designs. In designing DMFBs, each control pin is associated with an electrical pad for identifying an unique input signal [4, 11, 14]. By using a combinational logic, which is obtained by adding a signal inverter to form a complement function, a further pin-count reduction can be achieved (at most divide the pin count by 2) [3]. Specifically, each control pin is combined with means for generating, in addition to an input signal, a *complementary* signal. This feature makes it available to consider the compatibility between identical and complementary signals when applying the broadcast addressing. As the example in Figure 3(b), we can change the actuation sequence of pin 2 into "01100". Then, the actuation sequences of pin 1 and pin 2 form a complementary pair and thus can be further merged together. Consequently, the pin count can be reduced from 5 to 3 as shown in Figure 3(c). This reduction achieves much fewer electrical connections between the chip and control system and thus simplifies the practical fabrication and package design. Therefore, the derivation of a correct broadcast-addressing result considering the compatibility between identical and complementary signals is of great importance, especially in pin-constrained designs.

2.2 Power Consumption

Although broadcast addressing offers a promising alternative for pin-constrained designs, the internal power consumption incurred by redundant actuations has become a potential problem. As discussed in Section 2.1, the essence of broadcast addressing is identifying the compatibility among actuation sequences by replacing the don't care symbol "X" with "1" or "0". Since "X" is irrelevant to scheduled fluidic operations, once a bit "X" is replaced with "1" during signal merging and electrode grouping, a redundant actuation is incurred. In this paper, we refer to this kind of bit "1" in each outcome actuation sequence as *redundant actuation unit*, or RAU for short. Obviously, the broadcast-addressing result is not unique, implying different numbers of RAUs for different addressing results. In fact, each RAU represents an *extra* demand of high actuation voltage [10, 13]. In executing a bioassay, an addressing result with a higher number of RAUs thus has more power consumption. Therefore, to minimize the power consumption, it is desirable to derive an addressing result such that the induced number of RAUs can be minimized.

For example, in Figure 3(b), the power-oblivious broadcast-addressing result has 18 RAUs. While our power-aware broadcast addressing in Figure 3(c) provides an alternative with only 8 RAUs. This reduction achieves lower power consumption when executing a bioassay, which is especially crucial for many battery-driven applications, such as handheld devices for point-of-care diagnosis [15]. Furthermore, reducing the number of RAUs also slows down the dielectric breakdown for some electrodes, which is caused by frequently switching to high actuation voltages [1]. In this way, the system reliability can be improved. Thus, by minimizing the number of RAUs for lower power consumption, advantages such as longer battery lifetime and higher system reliability can be achieved. Therefore, in designing PDMFBs, it is desirable to minimize the number of RAUs for low power consumption when applying the broadcast addressing. Concerning this, the design convergence imposed by simultaneously minimizing the pin count and power consumption has become the most difficult design challenge.

2.3 Broadcast-Addressing Constraint

In broadcast addressing, if a single control pin is assigned to an electrode set, all the corresponding actuation sequences of these electrodes must be *mutually-compatible*. Note that the compatibility is examined for both identical and complementary signals.

2.4 Problem Formulation

The design problem for power-aware broadcast addressing can be formulated as follows.

Input: *An electrode set E_e and control information of these electrodes in the form of actuation sequences.*

Constraint: *Broadcast constraints should be satisfied.*

Objective: *Derive an electrode-addressing result while minimizing the number of control pins and RAUs.*

3. ALGORITHM

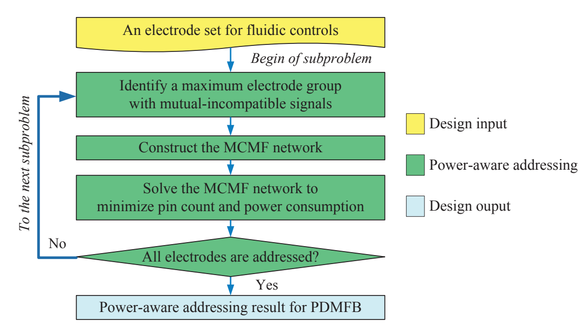

Figure 4: Overview of our algorithm.

Figure 4 shows the overview of our progressive network-flow based power-aware electrode-addressing algorithm. The essential intuition behind our algorithm is to reduce the design complexity by dividing the original problem into a set of manageable subproblems. In each subproblem, we identify a maximum electrode group with mutual-incompatible signals to facilitate the flow formulation. Then, pin-count and power-consumption minimizations are formulated to a minimum-cost maximum-flow (MCMF) network. By solving the flow network, we can optimally minimize the pin count and power consumption. Finally, iterations of subproblems end until all electrodes are addressed.

3.1 Compatibility Graph Construction

In applying broadcast addressing, an essential issue is grouping sets of electrodes such that all electrodes in the same group should be mutually-compatible. To specify this manner, a *compatibility graph* is constructed [13], where the vertex set represents the electrode set and an edge between two electrodes indicates their corresponding actuation sequences are compatible. Note that in this paper the compatibility is examined for both identical and complementary signals. Based on the compatibility graph, the electrode grouping can be mapped into the clique recognition problem [2, 13]. Although the clique recognition problem is a well-known example of an intractable problem in graph theory, many high quality heuristics and approximation algorithms are available in the literature to solve it efficiently [7].

3.2 Progressive Addressing Scheme

As modern high-integrated DMFBs usually contain hundred thousands of electrodes, it is inefficient to handle such a large flattened design during power-aware broadcast addressing. Motivated from [6], we propose a progressive addressing scheme based on *pin-count expansion* to remedy the deficiency. Figure 5 illustrates the overall idea behind the proposed method.

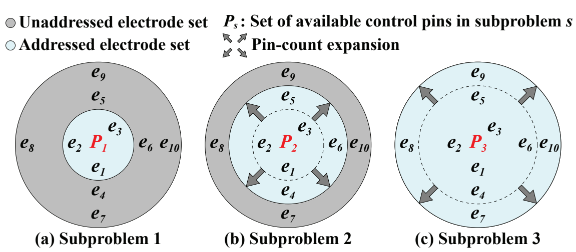

Figure 5: The concept of our progressive addressing scheme.

The main idea is to divide the original problem into a set of manageable subproblems corresponding to each pin-count expansion. After each expansion, the entire electrode set is decomposed into two subsets, an unaddressed electrode set and an addressed electrode set (see Figure 5(a)). Our addressing algorithm applies a network-flow based strategy to efficiently determine the minimum pin-count expansion for electrode addressing between the two subsets. Minimization of the number of RAUs is also considered in each pin-count expansion for low power consumption. Then, the pin count is progressively expanded and the addressing process seamlessly enters into the subsequent subproblem (see Figure 5(b)). Finally, expansion ends until all electrodes are addressed (see Figure 5(c)). Our progressive addressing scheme offers three major advantages as follows.

1. Instead of directly solving the original problem, we focus on each manageably-sized subproblem thereby reducing the entire design complexity significantly.
2. By constructing a flow network, the expansion of pin count can be minimally determined, as well as minimizing the number of RAUs for low power consumption.
3. Our progressive addressing also preserves the previously addressed result for the subsequent expansion, without numerous modifications of electrode readdressing.

3.2.1 Modeling the Pin-Count Expansion

The major challenge in our progressive addressing scheme is formulating the problem of pin-count expansion. The essence of pin-count expansion describes the concept of *extra* pin-count demand to realize the power-aware electrode addressing for each subproblem s. However, to avoid pin-count overhead, the expansion size must be minimized. Hence, the means by which the set of existing control pins in subproblem s, denoted as P_s, can be maximally utilized for addressing is the major concern in modeling the pin-count expansion.

The major difficulty in each subproblem s is to identify an unaddressed electrode set for addressing. The difficulty is the potential interference between grouping unaddressed electrodes with addressed ones without violating broadcast constraints. For example, as depicted in Figure 6(a), if we directly solve all the power-aware addressing problems between the addressed and unaddressed electrode sets, much of the compatibility needs to be examined for broadcast constraints and thus is computationally expensive. To tackle this problem, we reverse the regular electrode grouping method which is based on identifying the mutual compatibility. Specifically, we identify a maximum unaddressed electrode group, denoted as E'_e, with mutually *incompatible*, rather than compatible, control signals. As demonstrated in Figure 6(b), this strategy significantly reduces the complexity, which is attributed to the omission of grouping considerations inside E'_e. In this manner, the addressing problem can be regarded as a *one-to-one* matching determination between the two sets E'_e and P_s.

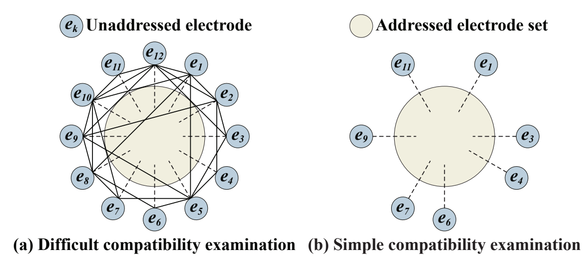

Figure 6: Compatibility between the unaddressed electrode set and the addressed electrode set. (a) Directly solves the power-aware electrode addressing with high design complexity. (b) Mutual incompatibility recognition ($E'_e = \{e_1, e_3, e_4, e_6, e_7, e_9, e_{11}\}$) with simple one-to-one matching.

After an unaddressed electrode group E'_e is identified, the major goal is to appropriately schedule an electrode-addressing result, while keeping the number of control pins and RAUs minimized. Since all electrodes $e_k \in E'_e$ must be independently addressed, unaddressed electrodes necessitate extra pin-count demand, implying a *pin-count expansion.* In order to avoid pin-count overhead, it is desirable to maximize the number of addressed electrodes by utilizing the existing control pins $p_j \in P_s$ such that the pin-count expansion can be minimized. Furthermore, the associated number of RAUs needs to be minimized during the addressing so as to minimize the power consumption. Consequently, for each subproblem s, the problem of pin-count expansion can be formulated as follows.

Given: *An existing control-pin set P_s, and a maximum unaddressed electrode set E'_e with mutual incompatibility.*

Constraint: *Broadcast constraints should be satisfied.*

Objective: *Maximize the number of addressed electrodes by using P_s such that pin-count expansion is minimized, while also minimizing the number of RAUs so as to minimize the power consumption.*

It should be noted that E'_e can be obtained by searching the maximum independent set of the compatibility graph, where we use the heuristic in [7] as the searching method.

3.2.2 Minimum-Cost Maximum-Flow Formulation

To minimize pin-count expansion while minimizing the number of RAUs, we construct a minimum-cost maximum-flow (MCMF) graph $G_{mcmf} = (V_{mcmf}, E_{mcmf})$ and propose two formulation rules. The first rule describes the formulation of V_{mcmf}, and the second rule describes the formulation of E_{mcmf}.

The key idea behind our MCMF formulation is to map the objective "*maximize the number of addressed electrodes by using P_s*" into "*maximum flow value*" in G_{mcmf}, with "*minimize the number of RAUs*" corresponding to "*minimum flow cost*". To avoid any violation of broadcast constraints in our MCMF formulation, we define the control pin set $P_s^k \in P_s$ for each electrode $e_k \in E'_e$, such that e_k can be addressed with a control pin $p_i \in P_s^k$. By identifying the compatibility of the actuation sequences between e_k and $p_j \in P_s$, the P_s^k can be obtained. Since the number of RAUs for addressing e_k with p_i should be minimized for low power consumption, we define the power cost for such an addressing as follows.

$$cost(e_k, p_i) = RAU_{e_k} + RAU_{p_i}, \forall e_k \in E'_e, p_i \in P_s^k \tag{1}$$

The $cost(e_k, p_i)$ represents the cost of addressing electrode e_k with control pin p_i and contains two parts, RAU_{e_k} and RAU_{p_i}. The first part represents the number of RAUs of e_k when addressing e_k with p_i. The second part represents the number of RAUs of those electrodes e'_k that are pre-addressed with p_i when addressing e_k with p_i. Note that the compatibility examination is based on the outcome actuation sequence of addressing e_k with p_i. With these definitions, the two MCMF formulation rules can be detailed as follows.

MCMF-Rule #1: Formulation of V_{mcmf}

1. For each electrode $e_k \in E'_e$, create a node v_{e_k}.
2. For each control pin $p_j \in P_s$, create a node v_{p_j}.
3. Create a source node s and a sink node t.

MCMF-Rule #2: Formulation of E_{mcmf}

1. For each node v_{e_k}, create a directed edge $s \rightarrow v_{e_k}$ with *one* unit capacity and *zero* cost per unit flow.
2. For each node pair (v_{e_k}, v_{p_i}), where $e_k \in E'_e$ and $p_i \in P_s^k$, create a directed edge $v_{e_k} \rightarrow v_{p_i}$ with *one* unit capacity and $cost(e_k, p_i)$ cost per unit flow.
3. For each node v_{p_j}, create a directed edge $v_{p_j} \rightarrow t$ with *one* unit capacity and *zero* cost per unit flow.

Based on the proposed MCMF formulation rules, we have the following two theorems.

THEOREM 1. *A feasible $s - t$ flow represents a correct electrode addressing without any violation of broadcast constraints.*

THEOREM 2. *Based on the proposed MCMF network, we can adopt the MCMF algorithm to optimally maximize the number of addressed electrodes with minimum total power costs.*

Based on the two theorems, we can maximize the number of addressed electrodes by deriving a maximum flow value in G_{mcmf} and have the following lemma.

LEMMA 1. *The extra pin-count demand for electrode addressing is equal to $|E'_e| - f_{mcmf}$, where f_{mcmf} denotes the maximum flow value in G_{mcmf}.*

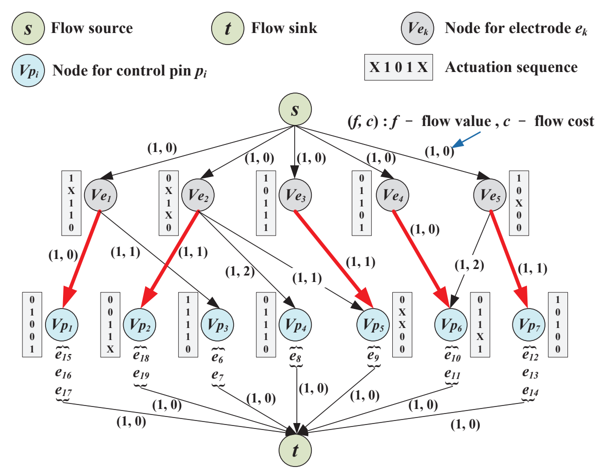

Figure 7: Illustration of the MCMF formulation for a subproblem s with $E'_e = \{e_1, e_2, e_3, e_4, e_5\}$ and $P_s = \{p_1, p_2, p_3, p_4, p_5, p_6, p_7\}$ by the proposed two flow formulation rules. After solving the MCMF network, we can obtain an electrode-addressing result as shown in the middle bold-red arrows $V_{e_k} \rightarrow V_{p_i}$.

We use Figure 7 to exemplify the MCMF formulation. This Figure shows an example for a subproblem s with an unaddressed electrode set $E'_e = \{e_1, e_2, e_3, e_4, e_5\}$ and an existing control pin set $P_s = \{p_1, p_2, p_3, p_4, p_5, p_6, p_7\}$. Referring to MCMF-Rule #1, we create a source node s and a target node t. Then, for each electrode $e_k \in E'_e$ and each pin $p_j \in P_s$, we create nodes v_{e_k} and v_{p_j}, respectively. There are also some electrodes that are pre-addressed with pin p_j. For example, electrodes $\{e_{15}, e_{16}, e_{17}\}$ are pre-addressed with pin p_1, as noted below the node v_{p_1}. Referring to MCMF-Rule #2, we establish the edge connections $s \rightarrow v_{e_k}$ and $v_{p_j} \rightarrow t$ for all nodes v_{e_k} and v_{p_j} with one unit capacity and zero cost per unit flow, respectively. Then, for each electrode e_k, we first identify the control pin set P_s^k such that e_k is addressable with these control pins. The control pin set P_s^k

can be found by examining the compatibility between the actuation sequences of e_k and p_j. For example, the control pin set of electrode e_1 is $P_s^1 = \{p_1, p_3\}$. After all control pin sets are found, we establish the edge connections $v_{e_k} \rightarrow v_{p_i}$ with one unit capacity and $cost(e_k, p_i)$ cost per unit flow, where $e_k \in E_e'$ and $p_i \in P_s^k$. The power cost $cost(e_k, p_i)$ represents the induced number of RAUs for addressing the electrode e_k with the control pin p_i. Take the $cost(e_2, p_2)$ for example. The outcome actuation sequence of addressing the electrode e_2 with the control pin p_2 consists of two parts, "00110" for e_2 and "00110" for $\{e_{18}, e_{19}\}$. Then, we can obtain $RAU_{e_2} = 1$ and $RAU_{p_2} = 0$. Thus, the power cost $cost(e_2, p_2)$ is summed up as 1. After adopting the same process for other nodes and edges, the entire MCMF network can be constructed, as shown in Figure 7. Next, we solve the entire flow network. As discussed before, the key idea behind our MCMF formulation is to map the objective "*maximize the number of addressed electrodes by using P_s*" into "*maximum flow value*" in G_{mcmf}, with "*minimize the number of RAUs*" corresponding to "*minimum flow cost*". This MCMF result shows that all the electrodes $e_k \in E_e'$ can be correctly addressed, implying *zero* size of pin-count expansion. Moreover, the minimum flow cost represents such an addressing result with totally minimum power costs (i.e., a minimum number of RAUs). Finally, we can trace the flow solution in the MCMF network to obtain the addressing result, as bold-red arrows depicted in Figure 7.

4. EXPERIMENTAL RESULTS

We implement the proposed algorithm in C++ language on a 2-GHz 64-bit Linux machine with 16GB memory. We evaluate our addressing algorithm on a set of real-life chip applications for amino-acid synthesis, multiplexed assay, and PCR amplification [8, 12, 13]. For comparison purpose, we implement the approach in [13], whose broadcast addressing is based on repeated clique recognitions and deletions. The statistics of all testcases and overall comparison results are listed in Table I. Note that all testcases can be solved within 1 second by both the implemented approach and proposed method.

TABLE I: COMPARISON BETWEEN [13] AND OURS

Assay	$\lvert E_e \rvert$	[13]		Ours	
		#Pin	#RAUs	#Pin	#RAUs
amino-acid	20	17	367	11	190
multiplexed	59	25	685	15	163
PCR	62	14	545	9	178
multi-functional	91	47	1563	30	239
Total		103	3160	65	770

#Pin: Pin count #RAUs: Number of redundant actuation units
$\lvert E_e \rvert$: Number of used electrodes

In the first comparison, we compare the pin count between [13] and our algorithm. As listed in Table I, since the typical broadcast addressing only considers the merging for identical signals, our algorithm, further considering the merging for complementary signals, thus reduces the pin count by 36.9%. This result shows that our addressing algorithm only requires a small number of control pins to perform the same fluidic functions, which achieves feasible fabrication, easy packaging, and low product cost. In the second comparison, we compare the number of RAUs between [13] and our algorithm. In executing the same fluidic functions, our addressing result achieves 75.6% reduction for the number of RAUs. This reduction shows that our addressing algorithm can greatly minimize the redundant actuations during signal merging and thus minimize the power consumption of PDMFBs. In this regard, the battery lifetime and system reliability can be greatly improved. Overall, the experimental results show that our algorithm leads to a superior addressing solution with lower pin-count demand and lower power consumption.

5. CONCLUSION

In this paper, we have proposed a novel network-flow based power-aware broadcast addressing for pin-constrained digital microfluidic biochips. The proposed algorithm is the *first* work in the literature that considers the power-consumption issue into broadcast addressing. A progressive network-flow based addressing scheme has been introduced to efficiently and correctly solve the entire design problem. By simultaneously minimizing the pin count and power consumption, our algorithm achieves higher integration and better design performance. Experimental results on real-life chip applications have demonstrated the effectiveness of our algorithm in terms of pin-count reduction and power-consumption minimization.

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